RISC-V Taiwan Alliance

（ since 2019 ）
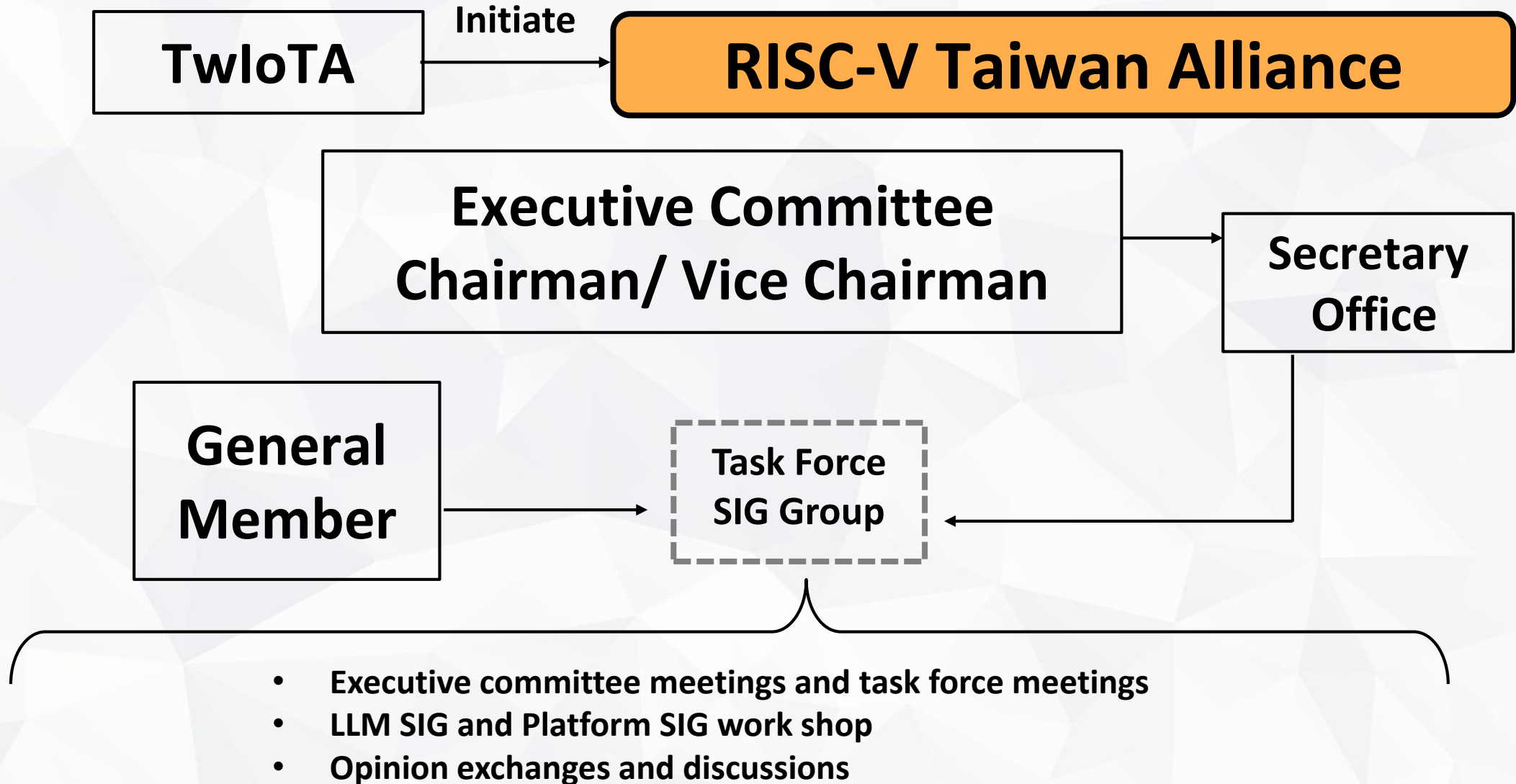
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About RISC-V Taiwan Alliance

Organization Structure

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TwIoTA  --Initiate-->  RISC-V Taiwan Alliance
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Executive Committee Chairman/ Vice Chairman → **Secretary Office**

General Member → **Task Force SIG Group** ← (Secretary Office)

- Executive committee meetings and task force meetings
- LLM SIG and Platform SIG work shop
- Opinion exchanges and discussions

Vision and Mission

RISC-V Taiwan Alliance (RVTA) is committed to coordinating industry, academy, and research institute to work together and introduce RISC-V open architecture to Taiwan.

Market

Technology

Talents
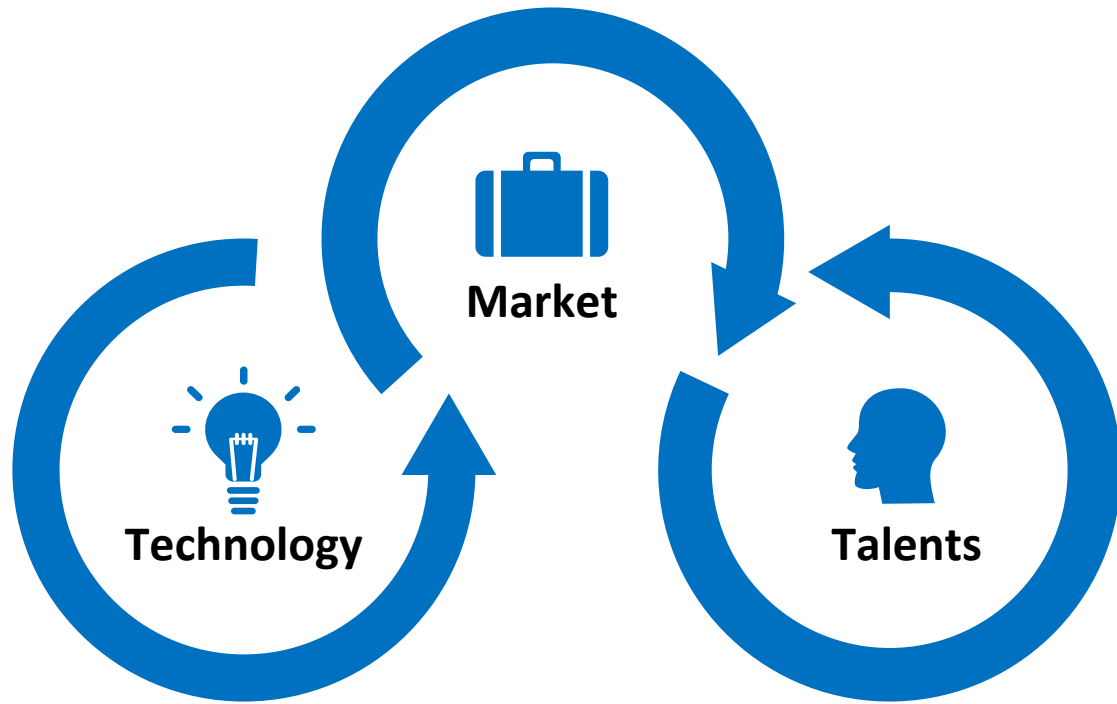
Technology
Promote RISC-V technology and accelerate the development of AIoT and edge computing industry in Taiwan.

Market
Support Taiwan's semiconductor business to enter the core customization of IC design and expedite the RISC-V open architecture into commercial market.

Talents
Cultivate and connect talent resources from RISC-V ecosystems worldwide, making Taiwan's ICT industry a key player in the global supply chain and core AIoT solution provider.
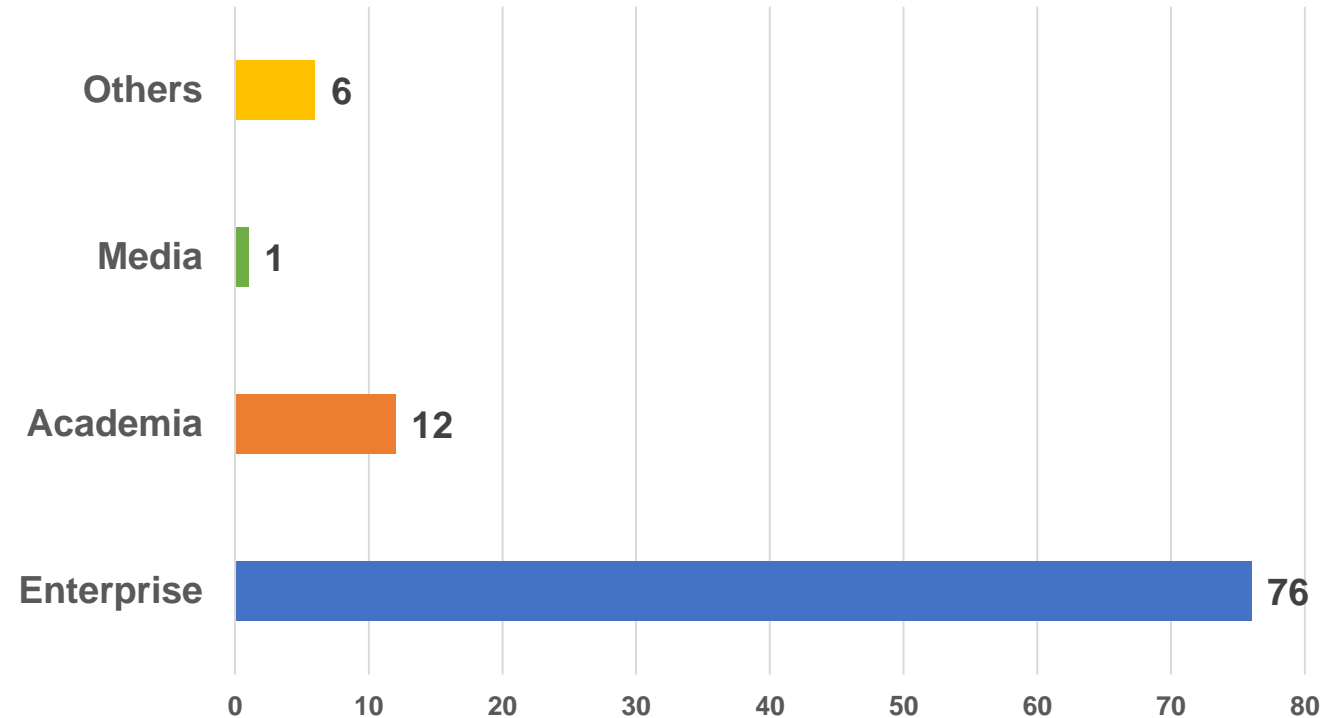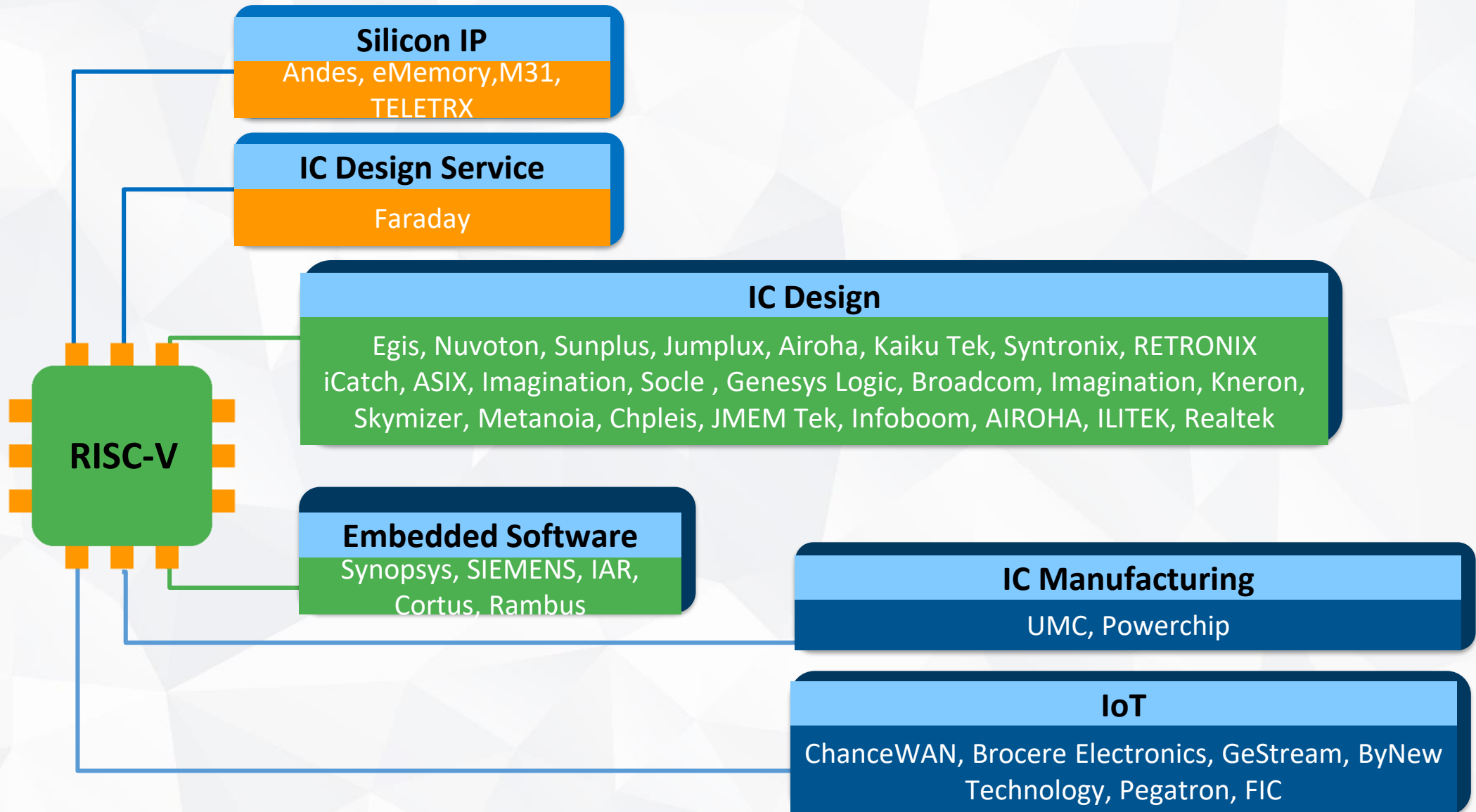
Current Member Status

Overall Membership	
Business	**Individual**
95	**407**

Business Member Breakdown

Category	Count
Others	6
Media	1
Academia	12
Enterprise	76

RISC-V Ecosystem of RVTA Members

Silicon IP
Andes, eMemory, M31, TELETRX

IC Design Service
Faraday

IC Design
Egis, Nuvoton, Sunplus, Jumplux, Airoha, Kaiku Tek, Syntronix, RETRONIX iCatch, ASIX, Imagination, Socle, Genesys Logic, Broadcom, Imagination, Kneron, Skymizer, Metanoia, Chpleis, JMEM Tek, Infoboom, AIROHA, ILITEK, Realtek

RISC-V

Embedded Software
Synopsys, SIEMENS, IAR, Cortus, Rambus

IC Manufacturing
UMC, Powerchip

IoT
ChanceWAN, Brocere Electronics, GeStream, ByNew Technology, Pegatron, FIC

Current Governance

Chairman

林志明 **Frankwell, Lin**

Chairman and CEO
Andes Technology

Vice Chairman

黃振昇
Jen-Sheng, Hwang
President, Syntronix

陳添福
Tien-Fu, Chen
Associate Dean / Professor, NYCU

Executive Committee

黃英哲	陳志成	李政崑	邱瀝毅	楊家驤	劉峻誠	盧俊銘	劉廣治
Ing-Jer, Huang	**Dr. Ryan Chen**	**Jenq-Kuen, Lee**	**Lih-Yih, Chou**	**Chia-Hsiang, Yang**	**Albert Liu**	**Jun-Ming, Lu**	**K.C. Liu**
Professor		**Professor**	**Professor**	**Professor**	**Chairman/Founder**	**Division**	**Executive VP**
NSYSU		**NTHU**	**NCKU**	**NTU**	**Kneron Taiwan**	**Director ITRI**	**Skymizer**

Functions and Responsibilities of RVTA EXCOs

Strategy
- Formulate the development strategies to ensure the operations align with the core objectives of promoting RISC-V technology.
- Define annual work plans and priorities to foster collaboration between industry and academia.

Member Service
- Safeguard the interests of RVTA members and adjust services based on needs.
- Organize member meetings, technical exchange forums, or workshops to promote collaboration and resource sharing among members.

Promotion
- Represent the alliance in relevant events to enhance the visibility of RVTA.
- Collaborate with government agencies, academic institutions, and industry partners to secure policy support and resources.

Management and Implementation
- Establish and implement internal management regulations to maintain transparency and fairness in alliance operations.
- Regularly review the alliance's charter and related regulations to ensure they meet member and external environmental needs.

Background and Milestone

Mar 7th , 2019
RVTA initiated and established by Taiwan IoT Technology and Industry Association

May 29th, 2019
RVTA hosted the RISC-V forum at COMPUTEX TAIPEI

Jul 30th & Sep 17th, 2019
RVTA co-hosted cross-strait standards forum in RISC-V section

Sep 25th, 2020
Named the RISC-V event in Taipei as RISC-V Taipei Day for the first time : RISC-V x Edge AI

Oct 12th, 2021
RISC-V Taipei Day : The Next Golden Decade of Future Computing Architecture

Sept 15th, 2022
RISC-V Taipei Day : Drive Into the Future with RISC-V Inside

Oct 12th, 2023
RISC-V Taipei Day: Unlocking the Possibilities of RISC-V in the AI Era

Sept 11th, 2024
RISC-V Taipei Day: Reshape the Future with AI

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2024 Events Highlights

- **4 EXCO meetings** (April 26, August 22, October 11, December 31) this year to decide on major alliance affairs and directions

- March 11: Established **2 SIGs** (Platform SIG, led by Ted Chang, Andes Technology; LLM SIG, led by Prof. TF Chen, NYCU)

- March 28: Participated in the **Andes RISC-V Con** in Hsinchu, setting up an alliance booth to promote membership.

- May 16: Attended the PQC Alliance Inaugural Meeting, forming a partnership to advance RISC-V technology in **post-quantum cybersecurity**.

- May 19: Signed a MoU with National Sun Yat-Sen University's "智慧電子晶片發展計畫" to **foster the chip design ecosystem in southern Taiwan**.

- August 9: Participated in the launch ceremony of the **Southern Taiwan Chip Design Industry Base**, organized by the Industrial Development Bureau, MOEA.

- September 11: Co-hosted "RISC-V Taipei Day" with DVCon Taiwan, **focusing on RISC-V and AI trends and applications**.

- October 16: **Platform SIG meeting** at the Kaohsiung Sun Yat-sen Industrial Development

- October 21-23: Attended the **RISC-V Summit North America** in Santa Clara, networking with RISC-V International experts and communities; prepared for inviting international speakers and sponsorships for 2025.

- November 15: Organized a **technical diffusion seminar and workshop** at NCKU.

- December 18: Participated in the Kaohsiung IC Design Ecosystem Forum, **with alliance member Kneron presenting on the relationship between NPU and RISC-V architecture**.

2024 Events Highlights

2024 RISC-V Taipei Day on September 11

Technical Diffusion Seminar and Workshop at NCKU on Nov. 15

Attending RISC-V Summit North America.

Membership Recruitment and Promotion

Alliance Website and Messaging

- **201** industry news articles, **50** trend insights, and **141** member updates have been published.
- The website's member database system is continuously being optimized."

02 | 2024 RISC-V Taipei Day

2024 RISC-V Taipei Day At a Glance

About RVTD

5 Keynotes | **5** Tech & Trends Presentations | **2** Panel Discussions
11 Demo Teams | **9** Sponsors | **4** Partners

Sponsor & Partner

Frankwell Lin

Chairman, RISC-V Taiwan Alliance

Chairman and CEO, Andes

Dr. Alex Wang

Chairman,

TwIoTA

Lu Dai

Board Chair

RISC-V International

Dr. Charlie Su

President and CTO, Andes

Wei-Han, Lien

Chief CPU Architect and Senior Fellow

Tenstorrent

Mark Hayter

Chief Strategy Officer & Co-Founder

Rivos Inc.

Dr. Ryan Chen

Advisor

MediaTek

Barna Ibrahim

Vice Chair

RISE Project

Ted Speers

Technical Fellow

Microchip

Travis Lanier

Chief Product Officer

Ventana

Prof. Tien-Fu, Chen

Professor, Dept. of Computer Science, National Yang Ming Chiao Tung University

Ted Chang

Spokesperson & Special Assistant

Andes Technology

Stewart Wu

Chairman, President and Chief Executive Officer

Metanoia Communications

Ming Chih

CEO

Chelpis Quantum

TIme	Topic	Speaker
9:00 - 9:30	Registration	
9:30 - 9:45	RISC-V: More Than AI	Frankwell Lin, Chairman, RISC-V Taiwan Alliance (Chairman & CEO, Andes)
9:45 - 9:50	Welcome Remark	Dr. Alex Wang, Chairman, TWIoTA
9:50 - 9:55	Welcome Remark	Chih-Ching Yang, Director General, IDA Ministry of Economic Affairs
9:55 - 10:00	Group Photo	
10:00 - 10:15	Architecture of Choice for AI	Lu Dai, Board Chair, RISC-V International (Senior Director of Technical Standards, Qualcomm)
10:15 - 10:35	Leveraging RISC-V Solutions for Intelligence Everywhere	Dr. Charlie Su, President and CTO, Andes Technology
10:35 - 10:55	Tech Talk 2	Wei-Han Lien, Chief CPU Architect and Senior Fellow, Tenstorrent
10:55 - 11:10	Using the RISC-V ecosystem to build System-on-Chips (SoCs) for Artificial Intelligence (AI) applications	Mark Hayter, CSO & Co-Founder, Rivos Inc.
11:10 - 11:30	Lunch/Exhibit Tour	
11:30 - 12:10	RISC-V Trend and AI	Moderator: Ryan Chen | Advisor, MediaTek Inc. Panelist: Lu Dai | Senior Director of Technical Standards, Qualcomm Technologies, Inc. Mark Hayter | Chief Strategy Officer & Co-Founder, Rivos Inc. Dr. Charlie Su | President and CTO, Andes Technology Wei-Han Lien | Chief CPU Architect and Senior Fellow Architecture | Tenstorrent

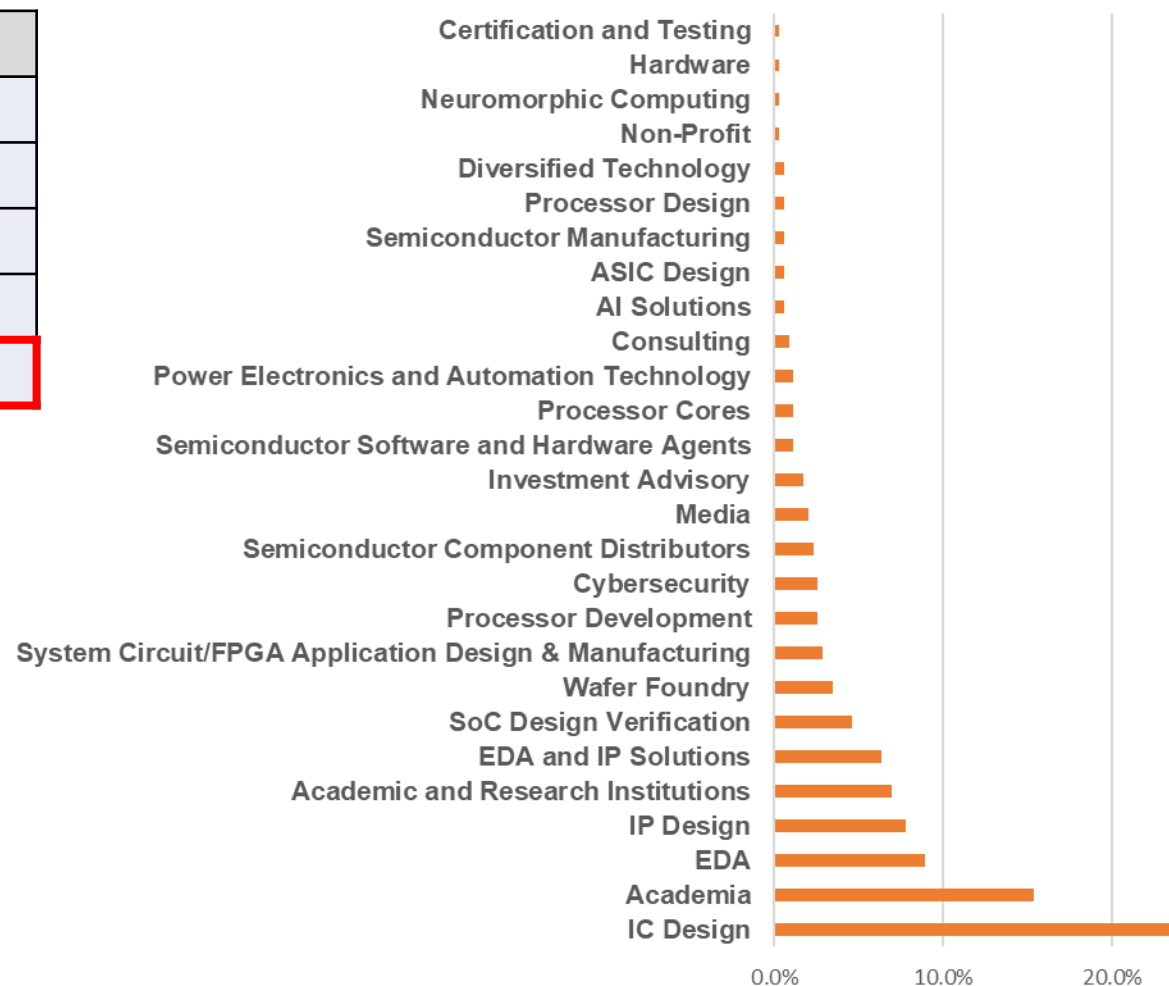| Time	Topic	Speaker
13:30 - 13:50	Empowering RISC-V Software: Strengths, Challenges, and Opportunities in Open Source Collaboration	Barna Ibrahim, Vice Chair, RISE Project
13:50 - 14:05	The Golden Age of Computer Architecture with MIcrochip and RISC-V	Ted Speers, Technical Fellow, Microchip
14:05 - 14:20	RISC-V Adoption: Powered by AI	Travis Lanier, Chief Product Officer, Ventana
14:20 - 14:40	Research Efforts of LLM SIG of RISC-V Taiwan Alliance	Prof. Tien-Fu, Chen | Vice Chair / SIG Convener, RISC-V Taiwan Alliance
14:40 - 15:00	Break / Lucky Draw 1	
15:00 - 15:20	Introduction of Platform SIG	Ted Chang | SIG Convener, RISC-V Taiwan Alliance (Spokesperson & Special Assistant, Andes Technology)
15:20 - 16:00	RISC-V Enable the AI Edge Everywhere	Moderator: Frankwell Lin | Chairman, RISC-V Taiwan Alliance Panelist: Ted Speers | Technical Fellow, Microchip Technology Travis Lanier | Chief Product Officer, Ventana Micro Systems Communications Inc. Stewart Wu | Chairman, President and Chief Executive Officer, Metanoia Communications Inc. Ming Chih | CEO, Chelpis Quantum Corp.
16:00 - 16:10	Break / Lucky Draw 2	
16:10 - 16:30	Closing and Networking	

>250 Participants in 2024

91.6% of Registration Rate

Category	Sign up	Register
Paid	77	63
PR	191	184
VIP	38	32
Press	6	7
Total	312	286

- Industry — 86.1%
- Research — 4.2%
- Academia — 5.5%
- ICF — 1.0%
- Press — 2.30%
- Other — 1.0%

Industry Type

- Certification and Testing
- Hardware
- Neuromorphic Computing
- Non-Profit
- Diversified Technology
- Processor Design
- Semiconductor Manufacturing
- ASIC Design
- AI Solutions
- Consulting
- Power Electronics and Automation Technology
- Processor Cores
- Semiconductor Software and Hardware Agents
- Investment Advisory
- Media
- Semiconductor Component Distributors
- Cybersecurity
- Processor Development
- System Circuit/FPGA Application Design & Manufacturing
- Wafer Foundry
- SoC Design Verification
- EDA and IP Solutions
- Academic and Research Institutions
- IP Design
- EDA
- Academia
- IC Design

0.0%   10.0%   20.0%

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RISC-V in the World

RISC-V International

RISC-V SUMMIT

THANK YOU TO 16.7K+ DEDICATED INDIVIDUALS

4,600 RISC-V Members across 70 Countries

Timeline values: 17 (2015), 46 (2016), 122 (2017), 210 (2018), 462 (2019), 1077 (2020), 2522 (2021), 3259 (2022), 4109 (2023), 4597 (Sep-24)

112 Chip — SoC, IP, FPGA

3 I/O — Memory, network, storage

22 Services — Fab, design services

54 Software — Dev tools, firmware, OS

4 Systems — ODM, OEM

**18 Industry** — Cloud, mobile, HPC, ML, automotive

**186 Research** — Universities, Labs, other alliances

4.2k Individuals — RISC-V engineers and advocates

Sep 2024 update

Source: RISC-V International

- **RISC-V SoCs is forecast to surpass 25% penetration by revenue and units in 2031**
- **Consumer (39%), Computer (33%), Automotive (31%), Data Center (28%), Industrial (27%), and Networking (26%) are projected to be the top Markets for RISC-V in 2031**

20B RISC-V SoCs, to Surpass 25% of Market
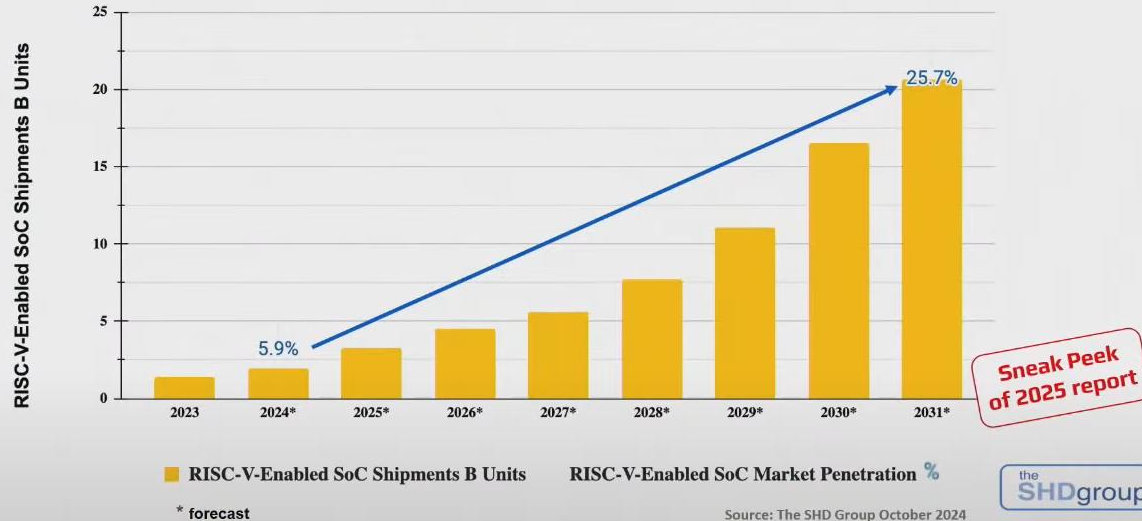
Top Markets for RISC-V 2031

Welcome to Join RVTA

https://www.twiota.org/RISC-V/member/JoinMember.aspx
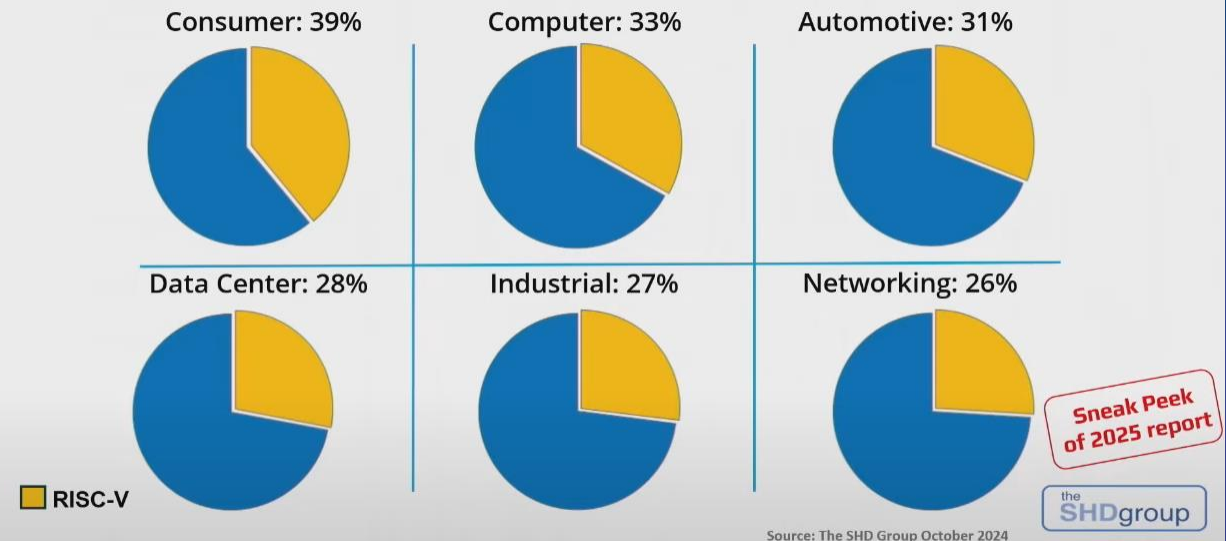
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