TSMC Showcases Leading Technologies at Online Technology Symposium and OIP® Ecosystem Forum

Hsinchu, Taiwan, R.O.C., Aug. 25, 2020 – TSMC (TWSE: 2330, NYSE: TSM) is showcasing the latest developments in its advanced logic technology, specialty technologies, 3DIC system integration solutions, and comprehensive design enablement ecosystem at the Company's first online Technology Symposium and Open Innovation Platform (OIP) Ecosystem Forum. TSMC brought its largest annual events online to maintain this important connection with customers and ecosystem partners during the global pandemic. More than 5,000 people registered for virtual events designed for North America, Europe, Japan, Taiwan, and China, held from August 24 to August 26.

"During these difficult times for communities around the world, people are relying on technology to communicate with and to comfort each other," said Dr. C.C. Wei, CEO of TSMC. "Our customer's innovations make the world a smarter and more connected place. TSMC is committed to unleashing our customer's innovations with the most advanced logic technologies, a full portfolio of specialty processes to bridge the physical and digital world, advanced packaging technologies, and a comprehensive set of system integration solutions."

Highlights of the Symposium include:

Advanced Technology Leadership – N5, N4, and N3

TSMC's industry-leading 5 nanometer (nm) N5 technology entered volume production this year and defect density reduction is proceeding faster than the previous generation as capacity continues to ramp. N5 provides a 15% performance gain or a 30% power reduction, and up to 80% logic density gain over the preceding N7 technology. Building on the original N5, TSMC plans to ramp an enhanced N5P version in 2021, offering an additional 5% speed gain and 10% power improvement.

TSMC also offered a preview of the latest member of the 5nm family – the N4 process. N4 will provide further improvements in performance, power and density to cover a wide range of product needs. In addition to process simplification with reduced mask layers, N4 also offers a straightforward migration path with the ability to leverage the comprehensive 5nm design ecosystem. The N4 process is scheduled to start risk production in fourth quarter of 2021, with volume production in 2022.

Looking ahead to the next generation, TSMC's N3 process is on track to become the most advanced logic technology in the world featuring up to 15% performance gain, up to 30% power reduction, and a logic density gain up to 70% over N5. With architectural innnovations, TSMC continues our technology leadership with a full-node advancement over the 5nm generation.

TSMC N12e™ Technology for Internet-of-Things in the 5G and AI Era

TSMC unveiled its N12e process, a technology now in risk production optimized for edge AI applications by providing both powerful computing performance and outstanding power efficiency. N12e brings TSMC's powerful FinFET transistor technology to edge devices enhanced with ultra-low leakeage (ULL) device and SRAM to deliver more than 1.75 times logic density improvement, and approximately 1.5 times performance improvement or less than half of the power consumption of the prior 22ULL generation of technology. An enhancement of the 12FFC+ process, N12e is ideal for AI-enabled IoT devices, giving them ample power to perform functions such as understanding natural speech or image classification while improving power efficiency. N12e also cuts the power cord and makes it possible to run powerful AI-enabled IoT devices on batteries. To learn more about the N12e process, please visit n12e.tsmc.com

TSMC 3DFabric™ System Integration Solutions

In addition, TSMC introduced 3DFabric, an umbrella of the company's fast-growing portfolio of 3DIC system integration solutions under one family of technologies that offer unparallelled flexibility for creating powerful systems through robust chip interconnections. With an array of options for both silicon stacking at the front end and packaging chips together at the back end, 3DFabric enables customers to connect logic dies together, to high-bandwidth memory (HBM) or to heterogeneous chiplets such as analog, I/O, and RF blocks. What's more, 3DFabric is the industry's first solution capable of combining back-end 3D and front-end 3D technologies for a powerful multiplier effect in system integration. TSMC's 3DFabric augments and complements transistor scaling for continuously improving system performance, functionality, slimming down form factors, and improving time-to-market.

3DFabric is comprised of TSMC's System on Integrated Chips (**TSMC-SoIC™**), Chip on Wafer on Substrate (**CoWoS®**), and Integrated Fan-Out (**InFO**) technologies.

About TSMC

TSMC pioneered the pure-play foundry business model when it was founded in 1987, and has been the world's largest dedicated semiconductor foundry ever since. The Company supports a thriving ecosystem of global customers and partners with the industry's leading process technologies and portfolio of design enablement solutions to unleash innovation for the global semiconductor industry. With global operations spanning Asia, Europe, and North America, TSMC serves as a committed corporate citizen around the world.

TSMC deployed 272 distinct process technologies, and manufactured 10,761 products for 499 customers in 2019 by providing broadest range of advanced, specialty and advanced packaging technology services. TSMC is the first foundry to provide 5-nanometer production capabilities, the most advanced semiconductor process technology available in the world. The Company is headquartered in Hsinchu, Taiwan. For more information please visit https://www.tsmc.com.

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