RISC-V Taiwan Alliance (RVTA) Update
While RVTA gathers industry and academia expertise, momentum of RISC-V is building up primarily by business and research opportunities.
Examples of RISC-V announcements

RISC-V Taiwan Alliance (RVTA)

<table>
<thead>
<tr>
<th>Foundry</th>
<th>IP</th>
<th>Design service</th>
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<tbody>
<tr>
<td>TSMC</td>
<td>Andes: Launches RISC-V FreeStart Program with its Commercial-Grade CPU N22.</td>
<td>Faraday: Unveils RISC-V ASIC Solution to Support Edge AI and IOT SoCs, proven in mass production.</td>
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** Highlight: Processing in Memory**

Powerchip forms AI Memory Corp. for solutions to the memory wall in computing.
Processing in Memory*

Unprecedented scalable ultra-efficient PIM* architecture and chip

Boosting 20x data intensive applications

4 Gb DRAM memory chips, embedding 8 processors on die

Power efficiency 10x better

Delivered as standard DDR4 2400 DIMM modules with 16 chips

By reducing drastically CPU-DRAM data movement

Server CPU helped by thousands of additional cores

At marginal cost

Source: HOT CHIPS 31, UPMEM 2019 Paper
RISC-V Application domain from edge to cloud

Andes V5 Adoption

Applications:

- ADAS
- AIoT at the edge
- Communication: BT, WiFi, 5G
- SSD: enterprise/consumer
- FPGA
- MCU
- Multimedia: A/V, AR/VR
- Block chain
- Datacenter AI accelerator
- Security
- FPGA
- MCU
- Multimedia: A/V, AR/VR

50% use AI
40nm to 7nm

Courtesy of: Andes Technology
RISC-V Application domain from edge to cloud

Andes just announced it achieved a record of 125 licensing agreements for its new family of RISC-V processors during the year of 2019 so far.
Contribution in Foundation Task Groups

RISC-V Taiwan Alliance (RVTA)
Contribution in software ecosystem

GNU Toolchains

RISC-V LLVM Porting Effort
- Alex Bradbury is in charge of RISC-V LLVM/M
  - Talk yesterday afternoon
  - Poster on Tuesday night
- RV32IM[AFJ]D support upstream
  - Missing half-precision floating point
  - Floating point is missing
- Clang, Go, and OpenJDK have run code
  - Rust port in progress
  - Poster on Tuesday

RISC-V Linux Kernel Port
- Linux: January, 2018
  - Only RISC-V based systems
  - Drivers are trickling in now

companies: ANDES, SiFive, bluespec, redhat, lowRISC, Berkeley, WD
RISC-V in University research is growing

RISC-V Taiwan Alliance (RVTA)

National Cheng Kung University
National Chiao Tung University
National Taiwan University
National Sun Yat-Sen University
National Tsing Hua University
RISC-V TAIWAN Alliance (RVTA) is committed to coordinating industry, academic, and research institute to work together and introduce RISC-V open architecture to Taiwan.

As soon as we connect resources from RISC-V ecosystems worldwide, Taiwan’s R&D, design and application will be capable of integrating AIOT and hitchhiking 5G trends and business opportunities, improving Taiwan’s industrial competitiveness.
Mission
RISC-V Taiwan Alliance (RVTA)

Market
Support Taiwan’s semiconductor business to enter the core customization of IC design and expedite the RISC-V open architecture into commercial market.

Technology
Promote RISC-V technology and accelerate the development of AIoT and edge computing industry in Taiwan.

Talents
Cultivate talents, and connect resources from RISC-V ecosystems worldwide, making Taiwan’s ICT industry a key player in the global supply chain and core AIoT solution provider.
What we have achieved

- Mar 7th, 2019
  RVTA was established

- May 22nd, 2019
  Chairman Wang visited MIIT in Beijing

- May 29th, 2019
  RVTA hosted the RISC-V forum at COMPUTEX TAIPEI

- Jul 30th & Sep 17th, 2019
  RVTA co-hosted cross-strait standards forum in RISC-V section
Community is a great force to advance technologies.

But, you must be able to work with it and tolerate its pace.
THANK YOU!

www.twiota.org/risc-v